



Advanced Digital VLSI Circuit Design



Indian Institute of Technology Jodhpur (IITJ), March 7-18, 2016

Overview

Today state of the art, complex System on a Chip (SoC), are capable of integrating few billion transistors on a substrate economically. At the same time, such circuits are produced in the fabrication plants that requires billions of dollars of investment. Therefore, circuit designers and architects must be aware of circuit as well as manufacturing challenges associated with it in order to design SoCs economically. In this course, the attendees will be exposed to advanced digital circuit concepts.

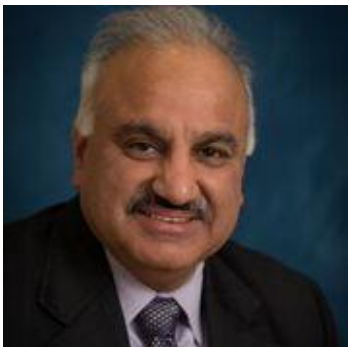
The primary objectives of the course are as follows:

- i) This is an advanced digital VLSI circuit design course that builds on a basic understanding of MOS transistor. Students will be exposed to the state on the subject matter.
- ii) Providing students hand-on training and skills to design and simulate circuits in labs.

You should attend if...

- you are a graduate student or an engineer interested in gaining an understanding of the VLSI circuit design.
- you are a researcher interested in developing skills to design and simulate circuits in lab.
- you are a research scientist or a young faculty interested in applying your circuit design concepts to produce them successfully.

The Faculty



Prof. Manoj Sachdev is a professor in the Electrical and Computer Engineering department, at the University of Waterloo, Canada. His research interests include low power and high performance digital circuit design, mixed-signal circuit design, test and manufacturing issues of integrated circuits. He has contributed to five books, book chapters, and has co-authored 200 technical articles in conferences and journals. He holds more than 30 granted and several pending US patents on various aspects of VLSI circuit design, reliability, and test, and has been consultant to several semiconductor companies.

Participation Fee#

- Participants from Abroad: USD 200
- Industry/Research organization: INR 5,000 /-
- Academic Institutions: INR 2000/-
- Number of participants will be limited to 30.

This include all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24 hr free internet facility.

Participation fee is in addition to the registration fee that is to be paid on the GIAN portal.

Course Co-ordinator

Dr. Suresh Gundapaneni
Phone: +91-291-2449074
E-mail: suresh@iitj.ac.in

.....
Course registration Link:
<http://www.gian.iitkgp.ac.in/GREGN>

Please email the registration confirmation and the shortlisted candidate would be notified via email through GIAN portal.